wherein the semiconductor chip is disposed over and coupled to the conductive path of the die pad shape through a thermally conductive material, and the conductive path of the external connection shape is coupled to said semiconductor chip through an insulating material.

18. (New) A semiconductor device according to claim 17, further comprising:

connecting means for electrically connecting said semiconductor chip to the conductive path of the bonding pad shape;

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19. (New) A semiconductor device according to claim 17, further comprising:

an insulating resin covering said semiconductor chip, filling in the trench, and integrally supporting the semiconductor chip and the conducive paths with a bottom surface of the paths exposed.

20. (New) A semiconductor device according to claim 17 wherein the conductive path of the die pad shape has a smaller size than that that of the rear surface of said semiconductor chip, the conductive path of the external connecting shape is larger than the conductive path of the bonding pad shape.

21. (New) A semiconductor device according to claim 20, wherein the insulating material is provided between said wiring extended to the rear surface of said semiconductor chip and said semiconductor chip or between the conductive path of the external connecting shape and said semiconductor chip.

22. (New) A semiconductor device according to claim 17, wherein the side of each of said conductive paths is curved to mate with said insulating resin.

23. (Amended) A semiconductor device according to claim 17, further comprising:

a conductive film selectively covering said conductive paths and having made of material selected from the group consisting of nickel, silver and gold.

24. (New) A semiconductor device according to claim 17, wherein the conductive path of the die pad shape is coupled with a conductive pattern formed on a mounting board through a thermally conductive material.

25. (New) A Semiconductor device comprising:

a semiconductor chip;

a conductive path comprising a first path extending under the semiconductor chip to form an external electrode and a second path extending from the first path and having a first face connected to the semiconductor chip and a second face provided as another external electrode.--

REMARKS

Claims 1 to 3 and 5 to 16 have been examined. New claims 17 to 25 have been added. These claims are based on the original claims, expect for claim 25, which is supported by, for example, Fig. 1 and the description in the specification. No new matter has been added. Thus, claims 1 to 3 and 5 to 25 are pending.

Applicants respond to the advisory action mailed July 3, 2002 as follows:

Claim Rejections – 35 USC §103

Claims 1 to 3 and 5 to 16 have been rejected as being unpatentable over Fukutomi et al. in view of Fjelstad and Kweon et al. No claims have been amended in this response. Applicants submit that the cited claims are unobvious for the following reasons.

Claim 1 recites as follows:

> 1. (Twice Amended) A semiconductor device comprising:
> a plurality of conductive paths electrically separated from one another by a trench;
> a first conductive path of said plurality of conductive paths, having a die pad shape;
> a semiconductor chip disposed over said first conductive path; **said first conductive path coupled to said semiconductor chip through a thermally conductive material**;